METHOD AND APPARATUS FOR ENHANCING THE PERFORMANCE OF A PIPELINED DATA PROCESSOR

ABSTRACT

A method and apparatus for enhancing the performance of a multi-stage pipeline in a digital processor. In one aspect, the stalling of multi-word (e.g. long immediate data) instructions on the word boundary is prevented by defining oversized or "atomic" instructions within the instruction set, thereby also preventing incomplete data fetch operations. In another aspect, the invention comprises delayed decode of breakpoint instructions within the core so as to remove critical path restrictions in the pipeline. In yet another aspect, the invention comprises a multi-function register disposed in the pipeline logic, the register including a bypass mode adapted to selectively bypass or "shortcut" subsequent logic, and return the result of a multi-cycle operation directly to a subsequent instruction requiring the result. Improved data cache integration and operation techniques, and apparatus for synthesizing logic implementing the aforementioned methodology are also disclosed.